## REMARKS

The Official Action mailed September 10, 2002 has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time.

Applicants note with appreciation the consideration of the Information Disclosure Statements filed on August 13, 1998; June 2, 1999; February 1, 2000; July 24, 2000; November 27, 2001; and May 17, 2002. Applicants note that the Information Disclosure Statements filed on October 24, 2000 and December 20, 2000 were only partially considered. In response, in a *Supplemental Response* dated May 31, 2002, the Applicants submitted the references missing from the Information Disclosure Statements filed on the October 24, 2000 and December 20, 2000. Unfortunately, the *Supplemental Response* did not include the correct Serial Number. In order to notify the Office of the proper Serial Number for the *Supplemental Response*, the Applicants representative contacted Marsha Richards, Customer Service Group 2800, sent a facsimile to Marsha Richards dated June 24, 2002, and sent a facsimile to the Examiner dated July 17, 2002. The Applicants respectfully request the Examiner's assistance in determining whether the references sent in the *Supplemental Response* have been received by the Examiner and entered into the file. If so, the Applicants further request consideration of those references and an indication of such consideration as appropriate.

A further Information Disclosure Statement is submitted herewith and careful review and consideration of this Information Disclosure Statement is requested.

Claims 1-3, 6, 7, 9, 10, 17-24, 26, 27, 30-33 and 36-55 are pending in the present application, of which claims 1, 7, 17, 21, 32, 36, 38 and 51 are independent. Claims 7, 17, 18, 46, 51, 54 and 55 have been amended herewith. For the reasons set forth in detail below, all claims are believed to be in condition for allowance.

Paragraph 2 of the Official Action rejects claims 7, 9, 10, 17-19, 27, 30, 51, 52 and 54 as anticipated by U.S. Patent No. 5,581,092 to Takemura. The Applicants respectfully submit that an anticipation rejection cannot be maintained against independent claims 7, 17 and 51 of the present invention, as amended. Takemura does not teach or suggest all the elements of the independent claims, either explicitly or

inherently. Specifically, independent claims 7, 17 and 51 have been amended to include a feature that a second substrate facing the first substrate with a gap therebetween, wherein the first substrate has an extended portion which extends beyond at least one side edge of the second substrate (Fig. 3). Also, this feature is recited in independent claim 38, which the Official Action has not rejected over Takemura. Since Takemura does not teach or suggest all the elements of the independent claims, either explicitly or inherently, an anticipation rejection cannot be maintained. Accordingly, reconsideration and withdrawal of the rejection of claims 7, 9, 10, 17-19, 27, 30, 51, 52 and 54 under 35 U.S.C. § 102(e) is in order and respectfully requested.

Paragraph 3 of the Official Action rejects claims 1-3, 6, 7, 9, 10, 17-24, 26, 27, 30-33 and 36-55 under the doctrine of obviousness-type double patenting over claims 3, 13 and 17 of U.S. Patent No. 5,889,291 to Koyama et al. As stated in MPEP § 804, under the heading "Obviousness-Type," in order to form an obviousness-type double patenting rejection, a claim in the present application must define an invention that is merely an obvious variation of an invention claimed in the prior art patent, and the claimed subject matter must not be patentably distinct from the subject matter claimed in a commonly owned patent. Also, the patent principally underlying the double patenting rejection is not considered prior art.

The Applicants respectfully traverse the obviousness-type double patenting rejection because independent claims 1, 7, 17, 21, 32, 38 and 51 of the present invention are patentably distinct from the claims of Koyama. Specifically, the independent claims of the present invention recite that the semiconductor integrated circuit chip is at least one of a memory, an input port, a correction memory, and a CPU. On the other hand, the claims of the Koyama patent merely recite a semiconductor chip and does not disclose or suggest that the chip is a memory, an input port, a correction memory, or a CPU. Although the specification of the Koyama patent recites that "a correction memory, a memory, a CPU, and an input port are chips that are mounted in such a manner," as stated above, the patent principally underlying the double patenting rejection is not considered prior art. Koyama does not claim a semiconductor chip

where the semiconductor chip is at least one of a memory, an input port, a correction memory, and a CPU.

Moreover, independent claim 36 recites that each of the first plurality of thin film transistors is a bottom gate type, and each of the second plurality of thin film transistors is a top gate type. The Koyama patent also does not claim this feature.

The Applicants respectfully submit that the subject application is patentably distinct from the Koyama patent. Reconsideration of the obviousness-type double patenting rejection is requested.

The subject application is believed to be in condition for allowance, however, should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact Applicant's undersigned attorney at the telephone number listed below.

Respectfully submitted,

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

IN THE CLAIMS:

Please amend claims 7, 17, 18, 46, 51, 54 and 55 as follows:

7. (Amended) A display device comprising:

a first substrate having a first surface;

an active matrix circuit including at least one thin film transistor formed over the first [surface of the] substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over the first [surface of the] substrate; [and]

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one semiconductor integrated circuit chip disposed over the first [surface of the] substrate and operationally connected to said driving circuit wherein said semiconductor integrated circuit chip is at least one of a memory, an input port, and a CPU,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first [surface of the] substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.

17. (Amended) An electric device comprising:

a first substrate having an insulating surface;

a plurality of thin film transistors formed on the insulating surface, said plurality of thin film transistors being formed from a common semiconductor film formed on said insulating surface; [and]

a second substrate facing said first substrate with a gap therebetween, said first substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one single crystalline semiconductor integrated circuit chip formed on the insulating surface wherein said semiconductor integrated circuit chip is at least one of a memory, an input port, a correction memory and a [CPU;] CPU,

wherein at least one of the thin film transistors is provided as an active matrix circuit, at least another one of the thin film transistors is provided as at least one driving circuit for driving the active matrix circuit and the semiconductor integrated circuit chip is provided as a control circuit for controlling the driving circuit, and wherein said common semiconductor film is formed by crystallizing a semiconductor film comprising amorphous silicon deposited on said insulating surface.

18. (Amended) The device of claim 17 wherein the first substrate comprises a glass substrate.

46. (Amended) The device according to claim 17 wherein said semiconductor integrated circuit chip is connected to a wiring comprising indium tin oxide formed over said first substrate.

51. (Amended) An electric device comprising:

[an] a first insulating substrate;

an active matrix circuit including at least one thin film transistor formed over [a first surface of] said first insulating substrate;

a driving circuit including at least another one thin film transistor for driving the active matrix circuit formed over said first [surface of the] insulating substrate; [and]

a second substrate facing said first insulating substrate with a gap therebetween, said first insulating substrate having an extended portion which extends beyond at least one side edge of the second substrate; and

at least one semiconductor integrated circuit chip disposed over said first [surface of the extended portion of the] insulating substrate and operationally connected with the driving circuit wherein said integrated circuit chip is at least one of a memory, an input port, a correction memory and a CPU,

wherein said at least one thin film transistor and said at least another one thin film transistor are formed from a common semiconductor film formed over the first [surface of the] insulating substrate, and

wherein said at least one thin film transistor of the active matrix circuit has at least one lightly doped drain between a channel region and a drain region thereof.

54. (Amended) The device of claim 51 wherein the first insulating substrate comprises a glass substrate.

55. (Amended) The electric device according to claim 51 wherein said semiconductor integrated circuit chip is connected to a wiring comprising indium tin oxide formed over said first insulating substrate.